REMARKS

Claims 8 through 24 and 28 through 37 are pending in this application. Claims 11, 19, 28, 31 and 34 are the independent claims. Claims 11 and 34 through 37 have been amended.

Claims 8 through 13, 15 through 24 and 28 through 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Blomgren et al., U.S. Patent No. 6,334,183.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren in view of Zuraski, Jr. et al., U.S. Patent Number 5,737,629.

Applicants have amended claims 11 and 34 through 37 to put them in better condition for allowance or at least in better form for consideration on appeal. Applicants respectfully traverse the rejections for the reasons set forth below.

35 U.S.C. § 102(e) Rejections

Claims 8 through 13, 15 through 24, and 28 through 37 are Patentable Over the Prior Art

Claims 8 through 13, 15 through 24 and 28 through 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Blomgren et al., U.S. Patent No. 6,334,183. Applicants respectfully traverse the Section 102 rejection. Claims 11, and 34 through 37 have been amended to put them in better form for allowance and the Applicants' previous remarks have been expanded upon to illustrate the deficiencies in the Blomgren et al. patent use in the Section 102 rejection.

Regarding claim 11 the Examiner states:

> Blomgren has taught a method for sub-register data operations for executing an instruction, the method comprising: executing the instruction on a first register and a second register; disabling a carryover of a result of the executed instruction from low-order bit positions of a result register to the high-order bit positions of the result register (Blomgren abstract, figure 2, column 9 line 64 – column 10 line 10; since the bits that are not involved in the addition are filled by the source registers previous value, the carryover bit is left out of the register when a value is passed through; however, when all of the bits of the operands are being added, a carry bit would be carried over the carry line from the each of the LOW and HIGH adders go on to the TOP adder, with the LOW's carry also going to the HIGH adder – this is required when adding all of the bits of the operands

together to calculate the correct value. – the carryover bit would only be disabled when the values are passed through to the result register, as shown in the table in figure 2) (See Office Action, paragraph 3, page 2.);

and merging a result of the executed instruction with a plurality of high-order bits from the first register, the plurality of high-order bits being copied into high-order bit positions from the first register, the plurality of high-order bits being copied into high-order bit positions of a result register, and the result being placed into low-order bit positions of the result register (Blomgren abstract, figure 2, column 9 line 64 – column 10 line 10; as shown in figure 2, when the add BX,AX->AX instruction is executed, the unchanged portion of the register is passed though while the result of the lower portion of the registers is calculated). (See Office Action, paragraph 3, bridging page 3.)

Claim 11 has been amended and now recites, *inter alia*:

executing the instruction on a first register and a second register;

disabling a carryover of a result of the executed instruction from low-order bit positions of a result register to high-order bit positions of the result register; and

merging the result of the executed instruction with a plurality of high-order bits from the first register, the plurality of high-order bits being copied into high-order bit positions of the result register, and the result being placed into the low-order bit positions of the result register.

Contrary to the Examiner's assertion, the Blomgren et al. patent does not disclose or suggest "disabling a carryover of a result of the executed instruction from low-order bit positions of the result register to high-order bit positions of the result register," as recited in claim 11. Instead, in the Blomgren et al. patent, and as described by the Examiner, "the bits that are not involved in the addition are filled by the source registers previous value, the carryover bit is left out of the register." (See Office Action, paragraph 15, page 5.) In other words, the carryover bit is either not generated (as in the mixed-alignment byte address - see Blomgren et al., column 11, lines 25 through 29), ignored or overwritten by the source register's previous value when it is passed to the result register. (See Blomgren et al., column 10, lines 2 through 10.) This is not the same as the affirmative recitation of "disabling a carryover of a result . . . " as recited in claim 11.

Likewise, the Examiner's assertion that "the carryover bit would only be disabled when the values are passed through the result register, as shown in the table in figure 2," does not anticipate "disabling a carryover of a result . . .," as recited in claim 11. The Examiner has misconstrued the operation of the LOW and HIGH adders in the Blomgren et al. patent. Specifically, at no time is the carryover "disabled," instead it is always enabled and the example(s) given by the Examiner just don't generate a carryover, i.e., passing through bits <7:0> from a single register or adding <7:0> zeros from one register to bits <7:0> from the other register. Thus, at no time is the carryover of either the LOW or HIGH adders ever "disabled," as recited in claim 11.

There is nothing in the Blomgren et al. patent that discloses or suggests "disabling a carryover of a result of the executed instruction from low-order bit positions of the result register to high-order bit positions of the result register," as recited in claim 11. Therefore, the Examiner has failed to establish a *prima facie* case of anticipation, since the Blomgren et al. patent fails to disclose or suggest "disabling a carryover of a result. . .," as recited in claim 11. Accordingly, the Section 102 rejection of claim 11 is believed to be overcome and claim 11, and claims 12, 13 and 15 through 18 that depend therefrom are believed to be allowable and Applicants respectfully request the Examiner withdraw the Section 102 rejection of claims 8 through 13 and 15 through 18.

Regarding claim 19, claim 19 recites, *inter alia*:

> the logic circuit including a carryover circuit to disable a carryover from the execution of the instruction to the unchanged portion of the destination register.

For at least those reasons given above for claim 11, the Section 102 rejection is believed to be overcome for claim 19, as well as claims 20 through 24 that depend therefrom. In addition, there is no "carryover circuit," as recited in claim 19, disclosed or suggested by the Blomgren et al. patent. Therefore, Applicants respectfully submit that the Examiner has again failed to establish a *prima facie* case of anticipation of claim 19, which is believed to be allowable. Accordingly, Applicants respectfully request that the Section 102 rejection of claims 19 through 24 be withdrawn.

Regarding independent claim 28, which contains similar recitations as in claim 11, for at least those reasons given above for claim 11, the Section 102 rejection is believed to be overcome for claim 28, as well as claims 29 through 30 that depend therefrom. Therefore, Applicants respectfully submit that the Examiner has again failed to establish a *prima facie* case of anticipation of claim 28, which is believed to be allowable. Accordingly, Applicants respectfully request that the Section 102 rejection of claims 28 through 30 be withdrawn.

Regarding independent claim 31, which is a machine-readable medium format claim containing similar recitations as claim 28, for at least those reasons given above for claim 11, the Section 102 rejection is believed to be overcome for claim 31, as well as claims 32 and 33 that depend therefrom. Therefore, Applicants respectfully submit that the Examiner has again failed to establish a *prima facie* case of anticipation of claim 31, which is believed to be allowable. Accordingly, Applicants respectfully request that the Section 102 rejection of claims 31 through 33 be withdrawn.

Regarding independent claim 34, which is a machine-readable medium format claim containing similar recitations as claim 11, for at least those reasons given above for claim 11, the Section 102 rejection is believed to be overcome for claim 34, as well as claims 35 through 37 that depend therefrom. Therefore, Applicants respectfully submit that the Examiner has again failed to establish a *prima facie* case of anticipation of claim 34, which is believed to be allowable. Accordingly, Applicants respectfully request that the Section 102 rejection of claims 34 through 37 be withdrawn.

In view of the foregoing, the Applicants respectfully submit that the Examiner has failed to meet the required burden of establishing a *prima facie* case of anticipation, since the Blomgren et al. patent fails to disclose each and every element of the currently pending claims. Therefore, claims 8 through 13, 15 through 24 and 28 through 37 are patentably distinguishable over the prior art of record.

Accordingly, Applicants believe that claims 8 through 13 and 15 through 24 and 28 through 37 are allowable over the applied art and respectfully request a notice of allowance to that effect be issued.

35 U.S.C. § 103(a) Rejections

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren et al. in view of Zuraski, Jr. et al., U.S. Patent Number 5,737,629. Applicants respectfully traverse the Section 103 rejection.

Regarding claim 14, for at least those reasons given above for claim 11, the Section 103 rejection is believed to be overcome for claim 14. Specifically, the Examiner's combination of the Blomgren et al. and Zuraski, Jr. et al. patents fails to meet the required burden of establishing a *prima facie* case of obviousness, since there is nothing in the Zuraski, Jr. et al. patent that makes up for the shortcomings in the Blomgren et al. patent. Therefore, the applied combination does not teach or suggest each and every claim element recited in claim 14 and Applicants respectfully submit that claim 14 is allowable. Accordingly, Applicants respectfully request that the Section 103 rejection of claim 14 be withdrawn and a notice of allowance of claim 14 be issued.

CONCLUSION

In view of the above remarks, Applicant respectfully submits that the present case is in condition for allowance or at least in better form for consideration on appeal, and again requests that the Examiner issue a notice of allowance to that effect for all currently pending claims.

Applicants authorize the Commissioner to charge any fees determined to be due under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayment to Deposit Account No. 11-0600.

The Examiner is invited to contact the undersigned at (202) 220-4263 to discuss any matter concerning this application.

Respectfully submitted,

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